REMARKS

In the Office Action, the Examiner noted that Claims 1-23 are pending in the application and that Claims 1-23 are rejected. By this response, Claims 1-23 continue without amendment. In view of the following discussion, Applicants submit that none of the claims now pending in the application are anticipated under the provisions of 35 U.S.C. §102. Thus, Applicants believe that all of these claims are now in condition for allowance.

I. Objections

The Examiner objected to claim 18, stating that "the use of the word 'for' in describing what actions the different sections perform renders the claim indefinite. It is unclear if the action is performed or not by the section." (Office Action, p. 2). Applicants respectfully disagree. It is common practice to recite an element for performing a particular function in an apparatus claim. Unlike a method claim, an apparatus claim does not recite actions (steps) and thus the question of whether an action is performed or not by the sections is not relevant. Claim 18 recites three structural elements, namely, an input section, an augmentation section, and a translation section. Each of these elements is configured to perform (capable of performing) a particular function. For example, the input section is configured to perform the function of providing electronic design data responsive to the electronic design. Such language in an apparatus claim is permissible and definite under the provisions of 35 U.S.C. §112. Accordingly, Applicants respectfully request that the objection to claim 18 be withdrawn.

II. Rejection Of Claims Under 35 U.S.C. §102

The Examiner rejected Claims 1-23 as being anticipated by Filseth (United States Patent 5,473,546, issued December 5, 1995). The Examiner also rejected claims 1-3, 6-8, and 10-23 as being anticipated by Wikle (United States Patent 5,610,832, issued March 11, 1997). The Examiner also rejected claims 1-23 as being anticipated by Bening (United States Patent 6,684,381, issued January 27, 2004). The rejections are respectfully traversed.

A. The Filseth Patent

Filseth teaches a process for flattening hierarchical descriptions of electronic circuits into flat descriptions. (Filseth, Abstract). Filseth, however, does not teach or suggest each and every element of Applicants' claim 1. Namely, Filseth does not teach or suggest translating an electronic design of an integrated circuit into a circuit description language representation. Exemplary circuit description languages include HDLs, such as VHDL or VERILOG. Filseth processes an electronic design to produce flattened design data as output. A representation of the output in Filseth is shown in FIG. 4. (See Filseth, col. 9, lines 60-63). The memory map data shown in FIG. 4 does not teach or suggest a circuit description language representation. There is no teaching or suggestion in Filseth that the flattened design data is a circuit description language representation of the circuit.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir. 1984). Since Filseth does not teach or suggest translating an electronic design of an integrated circuit into a circuit description language representation, Filseth does not teach each and every element of Applicants' claim 1. Accordingly, claim 1 is not anticipated by Filseth.

Independent claims 6, 11, 13, 15, 18, and 21 each recite, among other features, translation or production of a circuit description language representation of an electronic design of an integrated circuit. For the reasons discussed above, Applicants contend that Filseth also fails to anticipate claims 6, 11, 13, 15, 18, and 21. Claims 2-5, 7-10, 12, 14, 16-17, 19-20, and 22-23 depend, either directly or indirectly, from claims 1, 6, 11, 13, 15, 18, and 21 and recite additional features therefor. Since Filseth does not anticipate Applicants' invention as recited in claims 1, 6, 11, 13, 15, 18, and 21, dependent claims 2-5, 7-10, 12, 14, 16-17, 19-20, and 22-23 are also not anticipated and are allowable.

In view of the foregoing, Applicants contend that claims 1-23 are not anticipated by Filseth and, as such, fully satisfy the requirements of 35 U.S.C. §102. As such, Applicants respectfully request that the rejection of such claims be withdrawn.

B. The Wikle Patent

Wikle teaches creation of an electrical circuit model of an integrated circuit layout. (See Wikle, Abstract). Wikle, however, does not teach or suggest each and every element of Applicants' claim 1. Namely, Wikle does not teach or suggest translating an electronic design of an integrated circuit into a circuit description language representation. As discussed above, exemplary circuit description languages include HDLs, such as VHDL or VERILOG. Wikle processes an electronic design to produce data structures as output. A representation of the output in Wikle is shown in FIGs. 6A-C. (See Wikle, col. 6, lines 56-65). The data structures shown in FIGs. 6A-C do not teach or suggest a circuit description language representation. There is no teaching or suggestion in Wikle that data structures are circuit description language representations of the circuit. Since Wikle does not teach or suggest translating an electronic design of an integrated circuit into a circuit description language representation, Wikle does not teach each and every element of Applicants' claim 1. Accordingly, claim 1 is not anticipated by Wikle.

Independent claims 6, 11, 13, 15, 18, and 21 each recite, among other features, translation or production of a circuit description language representation of an electronic design of an integrated circuit. For the reasons discussed above, Applicants contend that Wikle also fails to anticipate claims 6, 11, 13, 15, 18, and 21. Claims 2-3, 7-8, 10, 12, 14, 16-17, 19-20, and 22-23 depend, either directly or indirectly, from claims 1, 6, 11, 13, 15, 18, and 21 and recite additional features therefor. Since Wikle does not anticipate Applicants' invention as recited in claims 1, 6, 11, 13, 15, 18, and 21, dependent claims 2-3, 7-8, 10, 12, 14, 16-17, 19-20, and 22-23 are also not anticipated and are allowable.

In view of the foregoing, Applicants contend that claims 1-3, 6-8, and 10-23 are not anticipated by Wikle and, as such, fully satisfy the requirements of 35 U.S.C. §102. As such, Applicants respectfully request that the rejection of such claims be withdrawn.

C. The Bening Patent

Bening teaches providing HDL regular expression support for module iteration and interconnection. In particular, regular expressions are used in a preprocessing process to automate generation of repetitive HDL code. (See Bening, Abstract). Bening, however, does not teach or suggest each and every element of Applicants' claim 1. Namely, Bening does not teach or suggest translating an electronic design of an integrated circuit into a circuit description language representation. That is, there is no translation between different circuit representations in Bening. Rather, Bening expands particular expressions in HDL code into additional HDL code. Expanding expressions in HDL code does not teach or suggest translation of an electronic design of an integrated circuit into a circuit description language representation. Accordingly, claim 1 is not anticipated by Bening.

Independent claims 6, 11, 13, 15, 18, and 21 each recite, among other features, translation or production of a circuit description language representation of an electronic design of an integrated circuit. For the reasons discussed above, Applicants contend that Bening also fails to anticipate claims 6, 11, 13, 15, 18, and 21. Claims 2-5, 7-10, 12, 14, 16-17, 19-20, and 22-23 depend, either directly or indirectly, from claims 1, 6, 11, 13, 15, 18, and 21 and recite additional features therefor. Since Bening does not anticipate Applicants' invention as recited in claims 1, 6, 11, 13, 15, 18, and 21, dependent claims 2-5, 7-10, 12, 14, 16-17, 19-20, and 22-23 are also not anticipated and are allowable.

In view of the foregoing, Applicants contend that claims 1-23 are not anticipated by Bening and, as such, fully satisfy the requirements of 35 U.S.C. §102. As such, Applicants respectfully request that the rejection of such claims be withdrawn.

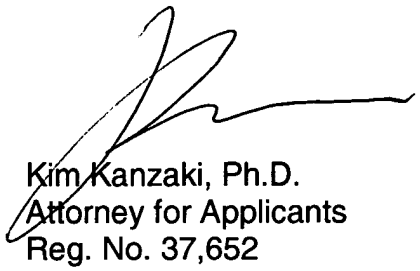
CONCLUSION

Thus, the Applicant submits that none of the claims presently in the application are anticipated under the provisions of 35 U.S.C. § 102. Consequently, Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring any adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Mr. Kim Kanzaki, Esq. at (408) 879-6149 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

Respectfully submitted,



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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on January 30, 2006..

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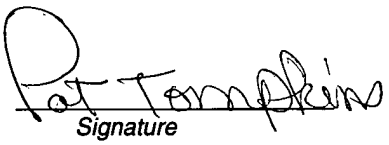

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